WHAT IS CLAIMED IS:

1. A method of processing successive input bits, comprising the steps of:

(a) providing:

(i) a RAM having a plurality of registers, each of said registers storing a word, all of said words being of equal length,

(ii) a shift register at least as long as any of said words, and

(iii) a pointer;

(b) initializing said pointer to point to one of said registers of said RAM; and

(c) for each group of j input bits shorter than said words:

(i) writing said word, stored in said register pointed to by said pointer, to said shift register,

(ii) shifting said word in said shift register by j bits,

(iii) writing said group of j input bits to said shift register, thereby producing an updated word in said shift register,

(iv) storing said updated word in said register pointed to by said pointer, and

(v) incrementing said pointer.

2. The method of claim 1, wherein j equals 1.

3. The method of claim 1, wherein all of said registers of said RAM are as long as each of said words.

4. The method of claim 1, wherein said shift register is as long as each of said words.

5. The method of claim 1, further comprising the step of:

(d) successively reading and processing at least some of said words stored in said registers of said RAM.

6. The method of claim 5, wherein all of said words stored in said registers of said RAM are read successively and processed.

Respectfully Submitted

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